CET2113C – Advanced Digital Circuits

Lab 3 – VHDL ALU's

Objective

The objective of the next two labs is to implement, in VHDL, all of the Standard combinational circuits that are used in the implementation of a simple Microprocessor. These include an ALU, Multiplexer, Comparator, Tri-State Buffer.

Part I: ALU

Using the ALU description in chapter 4 (along with the lecture notes), design, code, and test an ALU that implements the following functional table. First, please create the ALU using the dataflow model (i.e. create VHDL symbols for the HA, FA, LE, AE, CE and then connect them via schematics). Also, time how long it takes you to create the ALU using the dataflow model. After you have designed and tested the ALU using the dataflow model, recreate the ALU using the Behavior (i.e. Process Statement) model, and time how long that process takes:

s_2	s_1	s_0	Operation Name	Operation	x_i (LE)	y_i (AE)	c_0 (CE)
0	0	0	Pass	Pass A to output	a_i	0	0
0	0	1	AND	A AND B	a_i AND b_i	0	0
0	1	0	OR	A OR B	a_i OR b_i	0	0
0	1	1	NOT	A'	a_i'	0	0
1	0	0	Addition	$A + B$	a_i	b_i	0
1	0	1	Subtraction	$A - B$	a_i	b_i'	1
1	1	0	Increment	$A + 1$	a_i	0	1
1	1	1	Decrement	$A - 1$	a_i	1	0

Create a simulation for both ALUs, and show the simulation result to Dr. Poe for credit.

Q1) You designed the ALU in two different ways. Which took longer, and by how much?

Q2) If you were to construct the ALU in these two ways, which would have the better performance?